THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte RICHARD BEALKOWSKI

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Appeal No. 95-3517
Application 08/203,729[1]

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ON BRIEF

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Before MARTIN, BARRETT and FLEMING, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 6 and 8 through 20. Claim 7 pending in the

[1]Application for patent filed February 28, 1989. According to appellant, this application is a continuation of 07/705,277, filed October 30, 1990 (Paper No. 7, filed February 28, 1994). Appellant should note the correct filing date of 07/705,277 of May 24, 1991 and file an appropriate amendment to correct this error before issuance of patent.

application has not been rejected[2].

The invention is directed to a method and apparatus for extending a personal computer system's addressable physical memory space in a manner transparent to users of the address space.

The independent claim 1 is reproduced as follows:

> An apparatus for extending the address range of system RAM beyond the range of physical RAM, comprising:
>
> > a central processor, physical RAM having a fixed address range, and a bus for coupling the central processor to the physical RAM;
> >
> > secondary storage coupled to the bus;
> >
> > address decoder means for determining whether a read/write request for RAM is beyond the fixed address range of the physical RAM; and
> >
> > a secondary storage controller circuit, coupled to the bus, comprising:
> >
> > > a secondary storage manager to read/write emulated RAM on the secondary storage; and
> > >
> > > control means to determine the location of emulated RAM on the secondary storage and control reading and writing of emulated RAM by the secondary storage manager;
> > >
> > > whereby RAM storage addresses beyond the fixed address range of physical RAM addresses

[2]We note that on the first page of the final rejection, the Examiner states that claims 1 through 20 have been rejected. However, on pages 2 through 5 of the final action, claim 7 has not been included in any of the rejections.

> can be used by the processor, thereby extending the address range of the physical RAM.

The Examiner relies on the following references:

Christian et al. 4,403,288 Sep. 06, 1983

V. Carl Hamacher, "Computer Organization", second edition published by McGraw-Hill Company, 1984, pp. 214-216 & 313-317.

Claims 1, 5, 9, 13 and 17 stand rejected under 35 U.S.C. § 102 as being anticipated by Hamacher, sections 8.7 and 8.8. Claims 3, 11, 15 and 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hamacher, sections 8.7 and 8.8, in view of Christian. Claims 2, 4, 6, 8, 10, 12, 14, 16, 18 and 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hamacher, sections 8.7 and 8.8, in view of Christian and further in view of Hamacher, section 6.6.2.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1, 5, 9, 13 and

17 under 35 U.S.C. § 102 or the rejection of claims 2 through 4, 6, 8, 10 through 12, 14 through 16, 18 through 20 under 35 U.S.C. § 103.

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. ***See In re King***, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and ***Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co***., 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). "Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention." ***RCA Corp. v. Applied Digital Data Systems, Inc.***, 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.), *cert. dismissed,* 468 U.S. 1228 (1984), *citing* ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 772 218 USPQ 781, 789 (Fed. Cir. 1983).

On page 2 of the answer, the Examiner refers back to the final action for the grounds of the rejection. On page 2 of the final action, the Examiner relies on one sentence found on pages 313-314 of Hamacher that states:

> The mechanism that operates on these virtual addresses and translates them into actual locations in the physical hierarchy is usually implemented by a combination of hardware and software components.

The Examiners argues that the "combination of hardware and software" constitutes the secondary storage controller as claimed.

On pages 3-6 of the brief, Appellant argues that Hamacher fails to disclose a secondary memory controller to extend the effective memory space of system RAM as recited in Appellant's claims and thereby does not anticipate Appellant's claims 1, 5, 9, 13 and 17. In particular, Appellant points out that the cited sections of Hamacher are completely devoid of any teaching of an adaptor or controller as recited in Appellant's claims.

We note that Appellant's claims each recite the claim limitation directed to a secondary memory controller to extend the effective memory space of RAM. The Examiner is requesting us to speculate that Hamacher's statement referring to a mechanism that operates to translate virtual addresses by a combination of hardware and software components teaches a mechanism that would require the apparatus as claimed by Appellant. We do not wish to

do so. We note that such a combination of hardware and software does not necessarily require the apparatus as recited in Appellant's claims. In fact, we note that the translation is normally done by only the central processor and not by providing the additional hardware for such functions.

We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a ***prima facie*** case. ***In re Knapp-Monarch Co.***, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); ***In re Cofer***, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Therefore, we will not sustain the Examiner's rejection under 35 U.S.C. § 102.

In regard to the 35 U.S.C. § 103 rejection, the Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by

implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied,*** 117 S.Ct. 80 (1996), ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

The Examiner relies on Hamacher for a teaching of a secondary memory controller to extend the effective memory space of RAM. As we have found above, we fail to find that Hamacher teaches the structure as recited in Appellant's claims. Furthermore, we fail to find any suggestion in Hamacher or Christian to provide such structure. Therefore, we will not sustain the Examiner's rejection under 35 U.S.C. § 103.

We have not sustained the rejection of claims 1, 5, 9, 13 and 17 under 35 U.S.C. § 102 or the rejection of claims 2 through 4, 6, 8, 10 through 12, 14 through 16, 18 through 207 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

JOHN C. MARTIN Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MICHAEL R. FLEMING Administrative Patent Judge	)	

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